SPECIFICATION AMENDMENTS

Insert paragraph at page 1, between line 8 and 9:

This disclosure is a division of U.S. patent application 10/093,417, which is a continuation-in-part of U.S. patent application number 09/919,875 filed August 2, 2001.

Replace the paragraph beginning at page 1, line 16 with:

A semiconductor device is constituted of, for example, a semiconductor substrate made of a group IV ~~compound~~ element such as silicon or a group III-V compound semiconductor such as gallium arsenide (GaAs). Via holes are formed to penetrate through a semiconductor substrate so as to feed power to a semiconductor substrate of a completed semiconductor device or so as to impart the ground potential to the semiconductor substrate. The interior surface of each of the via holes is often plated with gold (Au) or the like. Processes of manufacturing the semiconductor device include ~~a plating process of~~ plating a semiconductor wafer before the wafer is ~~sliced~~ diced into a plurality of semiconductor chips. In each of the semiconductor chips, a via hole is formed. In the plating process, a plating layer is formed on the interior surface of each of the via holes while one of the ends of each via hole is closed; that is, each of the via holes is ~~held as~~ a blind hole.

Replace the paragraph beginning at page 5, line 16 with:

Figs. ~~4(a)~~ 4A and ~~4(b)~~ 4B show a plating layer formation step of a chemical processing method (or a plating method) of the present invention.

Replace the paragraph beginning at page 5, line 18 with:

Figs. ~~5(a)~~5A through ~~5(d)~~5D show an another embodiment of a chemical processing method (or plating layer formation method) in the present invention.

Replace the paragraph beginning at page 7, line 19 with:

Figs. ~~4(a)~~4A and ~~4(b)~~4B show a plating layer formation step of a plating method for plating the member 50 through use of the plating system according to the first embodiment, to thereby form a plating layer. Figs. ~~4(a)~~4A and ~~4(b)~~4B also show a plating process of a

method of manufacturing a semiconductor device. The member 50 which is to undergo the plating process corresponds to, e.g., a semiconductor wafer. The member 50 includes a semiconductor substrate 51 formed from, e.g., silicon or gallium arsenide. The semiconductor substrate 51 includes a plurality of semiconductor substrate portions. Figs. ~~4(a)~~4A and ~~4(b)~~4B show two semiconductor substrate sections 51A and 51B separated from each other by means of a phantom line. In a completed semiconductor device, the semiconductor substrate portions 51A and 51B are separated individually from each other along the phantom line. The thus-separated semiconductor substrate portions 51A and 51B are to become semiconductor substrates of respective semiconductor devices, the substrates being called chips. Reference numeral 60 designates a plating fluid.

Replace the paragraph beginning at page 8, line 13 with:

A thin feeding layer 54 is formed beforehand on the top of the semiconductor wafer 50, including interior surfaces 53a of the blind holes 53. A cathode potential is applied to the feeding layer 54 from the cathode contact 124. Consequently, a plating layer 70 is formed on the feeding layer 54. After completion of the plating operation, the bottom of the semiconductor wafer 50 is eliminated by means of, e.g., abrasion, until the respective via holes 52 become through holes. As shown in Figs. ~~5(a)~~5A through ~~5(d)~~5D, when via holes are formed after the semiconductor wafer 50 has been made thin, the semiconductor wafer 50 is made thin before formation of via holes through abrasion.

Replace the paragraph beginning at page 8, line 23 with:

Even in the face-up plating system, air bubbles 61 sometime develop and remain in the blind holes 53. In relation to the semiconductor wafer 50 in which via holes having a high aspect ratio are formed, the width of the blind hole 53 becomes smaller and the depth of the same becomes greater. Hence, there is increased the risk of the air bubbles 61 developing and remaining in the blind holes 53. In Fig. ~~4(a)~~4A, an air bubble 61 develops in a left-side blind hole 53. If the air bubble 61 remains during a plating operation, a plating failure 71 arises, as shown in Fig. ~~4(b)~~4B.

Replace the paragraph beginning at page10, line 16 with:

The second embodiment shows plating processes of the method of manufacturing a

semiconductor device. The second embodiment employs a semiconductor wafer 50A in which one end of each of the blind holes 53 is partially covered with a cover member. Figs. ~~5(a)~~5A through ~~5(d)~~5Dhow processes of producing the semiconductor wafer 50A having such blind holes 53; namely, processes ranging from a plating preparation process to a plating process.

Replace the paragraph beginning at page10, line 23 with:

Fig. ~~5(a)~~5A shows a first preparation step. In this step, cover members 55 formed from gold (Au) are bonded to a lower surface—namely, at predetermined areas on the back surface—of the semiconductor substrate 51, which is formed from, e.g., gallium arsenide (GaAs), and has a thickness ranging from 30 micrometers to 150 micrometers. The cover members 55 are attached to respective positions in which via holes 52 are to be formed. Fig. ~~5(b)~~5B shows a second preparation step, wherein a resist film 56 is formed on the upper surface of the semiconductor substrate 51. Openings 56a are formed at positions on the resist film 56 where the via holes 52 are to be formed. The semiconductor wafer 50A is etched in this state, whereby the via holes 52 are formed. The via holes 52 are formed so as to penetrate through the semiconductor substrate 51. Lower-end openings of the respective via holes 52 are closed by the cover members 55, thereby constituting the blind holes 53. Fig. ~~5(c)~~5C shows a third preparation step, in which the resist film 56 is removed and a thin feeding layer 54 is formed on the upper surface of the semiconductor substrate 51, including interior surfaces 53a of the blind holes 53. The feeding layer 54 corresponds to a thin film which is formed from, e.g., nickel (Ni)/gold (Au), titanium (Ti)/gold (Au), or chromium (Cr)/gold (Au), by means of sputtering or electroless plating.

Replace the paragraph beginning at page11, line 4 with:

Fig. ~~5(d)~~5D shows a plating process. A plating layer 70 made of, e.g., gold (Au), is formed in the processing chamber 130 of the closed plating cup 10. During the plating process, the semiconductor substrate 51 is plated while the openings of the blind holes 53 are oriented upward and remain in contact with the plating fluid circulating through the processing chamber 130. A pulsating pump is used as the pump 30, and the pressure and flow rate of the plating fluid in the processing chamber 130 vary in accordance with a pulsating cycle of the pulsating pump, thereby preventing any air bubbles 61 from remaining.

Replace the paragraph beginning at page 11, line 13 with:

A method of manufacturing a printed board is also identical with that shown in Figs. ~~5(a)~~5A through ~~5(d)~~5D. A printed board is formed from a dielectric board. A predetermined circuit pattern is formed from a copper layer on each of a pair of principal planes. Simultaneously, through holes are formed in predetermined areas so as to penetrate through the dielectric board. With the through holes being taken as blind holes, the printed board is plated in the same manner as shown in Fig. ~~5(d)~~5D. Eventually, plating layers provided on the interior surfaces of the through holes electrically interconnect predetermined circuit patterns provided on the respective principal planes. More specifically, the printed board is plated in the processing chamber 130 of the closed plating cup 10 while being oriented upward, such that the through holes formed in the board are opened at one end and closed at the other end, like the blind hole shown in Fig. ~~5(c)~~5C. Any air bubbles that remain in the blind holes are effectively discharged by means of pulsating action of the pump 30, thereby lessening the likelihood of plating failures. By means of the method for lessening the likelihood of plating failures, a manufacturing yield of a print board is improved, or the performance of a printed board is improved.